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APPLICATION BULLETIN
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VOLTAGE-TO FREQUENCY CONVERTERS OFFER USEFUL OPTIONS IN A/D CONVERSION

Specialized Counting Techniques Achieve Improved Speed and Resolution

Voltage-to-frequency converters (VFCs) provide unique characteristics when used as analog-to-digital (A/D) converters. Their excellent accuracy, linearity, and integrating input characteristics often provide performance attributes unattainable with other converter types. By using efficient frequency counting techniques, familiar speed/accuracy tradeoffs can be averted.

Since an analog quantity represented as a frequency is inherently a serial data stream, it is easily handled in large multichannel systems. Frequency information can be transmitted over long lines with excellent noise immunity using low cost digital line transmitters and receivers. Voltage isolation can be accomplished with low cost optical couplers or transformers without loss in accuracy. Many channels of frequency data can be efficiently steered to one counter circuit using simple digital gating, avoiding expensive analog multiplexing circuitry.

Like a dual-slope A/D converter, the VFC possesses a true integrating input. While a successive approximation A/D converter takes a "snapshot" in time, making it susceptible to noise peaks, the VFC's input is constantly integrating, smoothing the effects of noise or varying input signals. When system requirements suggest the VFC as an appropriate choice, a frequency measurement technique must also be chosen which meets the conversion speed requirements.

While it is clearly not a "fast" converter, conversion speed of a VFC system can be optimized by using efficient counting techniques.

The frequency counting scheme shown in Figure 1 is the most commonly used technique for converting the output of a VFC to a numerical quantity. A gate time is created by dividing a reference frequency down to a suitable period, T. The output pulses of the VFC are simply accumulated during the time the gate signal is high. If T is equal to one second, for instance, the output count M is equal to the VFC frequency. Other gate periods (often 0.1 seconds, 10 seconds, etc.) are conveniently scaled by a decimal point shift or a simple multiplying factor. The reset circuitry which must be used to clear the counter before the next gate period occurs is not shown in this simplified diagram.

Since the gate period is not synchronized to the VFC output pulses, there is a potential counting inaccuracy of plus or minus one count on M. This is easily seen by imagining a sliding window of width T along the VFC output waveform.

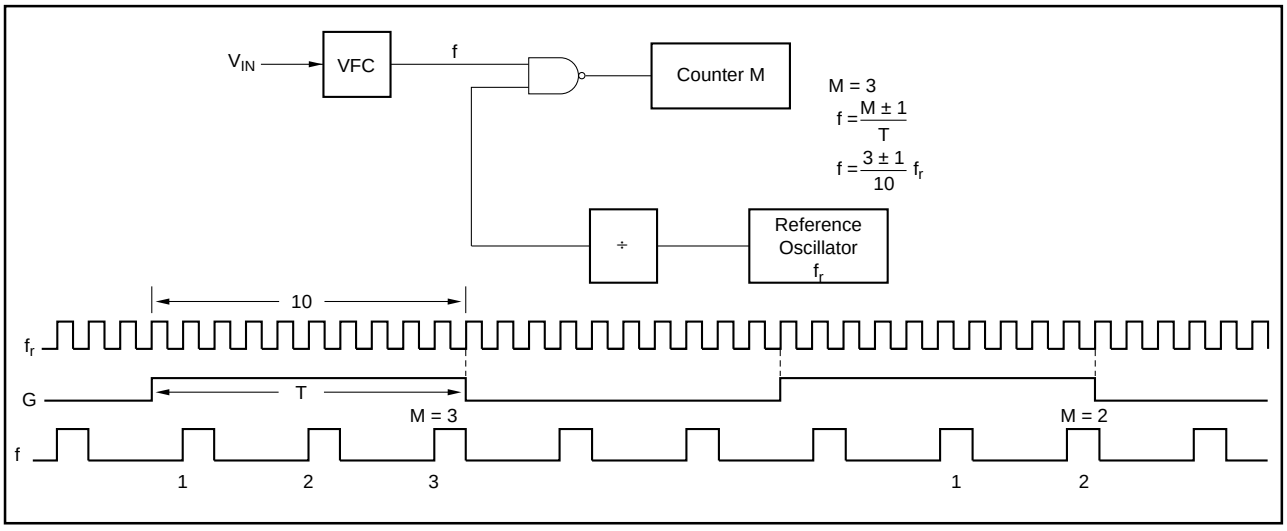

FIGURE 1. This Simplified Diagram of the Standard Counting Method Shows the Potential Inaccuracies That Can Occur. Although the first gate counts three rising edges of the VFC output frequency, f, the second gate period counts only two.

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Counting the rising edges which are seen in that period, you can see how, depending on the VFC frequency, a + one count error can occur.

The resolution which can be achieved by this method is related to the gate period, T, times the full-scale frequency of the VFC. This is equal to the number of counts, M, at full scale. Many applications require relatively fast conversions (short gate periods) with high resolution. This can only be accomplished by the use of a high full-scale frequency. This is an effective solution in many cases, but since VFC linearity degrades at high operating frequency, this often limits the available accuracy.

The ratiometric counting technique shown in Figure 2 (sometimes called reciprocal counting) eliminates this tradeoff. By counting N counts of a high speed clock which occur during an exact integer M counts of the VFC, an accurate ratio or the unknown VFC frequency to the reference (f_R) is determined.

This is accomplished by using a D flip-flop clocked with the VFC output. A new, synchronized gate period is created which is an exact number of VFC pulses in duration. In contrast to the standard counting approach which has a plus or minus one count error on M, the synchronized gate precisely counts an integer number of VFC pulses. During the same synchronized gate period, high speed clock pulses are counted. Since these high speed clock pulses are not synchronized with the gate, this count has a plus or minus one count error. High resolution is achieved by making the reference oscillator a high frequency so the N count is a large number. The one count error can then be made to have a small effect on the result.

The additional resolution of this counting technique means that for a given conversion speed, the VFC can now be operated at a low frequency where its linearity and temperature drift are excellent. Again, reset and control circuitry have not been shown to clearly illustrate the fundamentals of the technique.

The resulting two counts (M and N) are divided to achieve the result of an individual conversion. This can be done in a host processor or microcontroller along with the offsetting and scaling that often must be performed.

An example of a A/D system design using a VFC is shown in Figure 3. It uses a VFC110 to convert a 0 to 10V input into a 10kHz to 100kHz output by offsetting the VFC input with a reference voltage. The 5V reference sets a constant input current through R_1 which is added to the signal input current through R_{IN}. Since the synchronized gate awaits complete cycles of the VFC to achieve an exact count, a very-low VFC frequency would cause the synchronized gate period to be excessively long. The offset at the VFC input allows 10kHz (corresponding to 0V input) to be counted during the desired conversion time.

All counter functions are provided by a type 8254 counter/timer peripheral component which interfaces to many popular microprocessor systems. It contains three 16-bit counters which can be programmed for a variety of functions. Counter C2 provided the timing necessary to generate the gate signal "G". A rising logic edge at the Convert input initiates the conversion cycle. This causes FF1 to latch "high" Counter. C2 is programmed and loaded to count 59,667 clock pulses (3.58MHz clock), then reset FF1. This creates a 16.66ms(1/60s) gate period at "G". FF2 synchronizes the gate signal

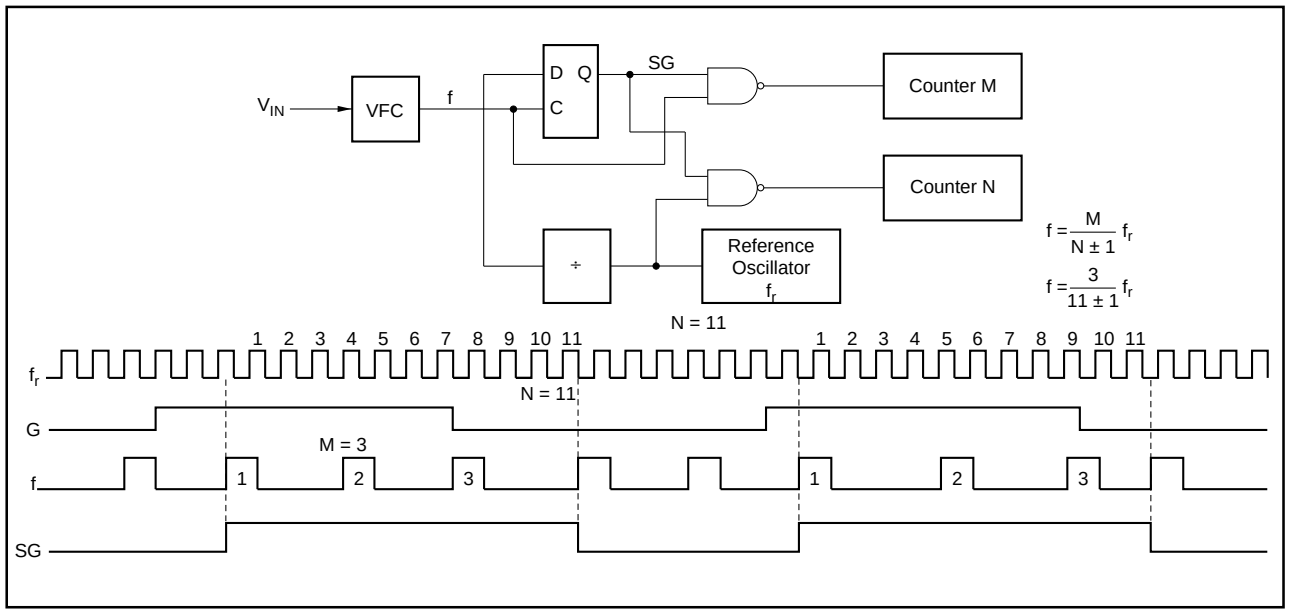
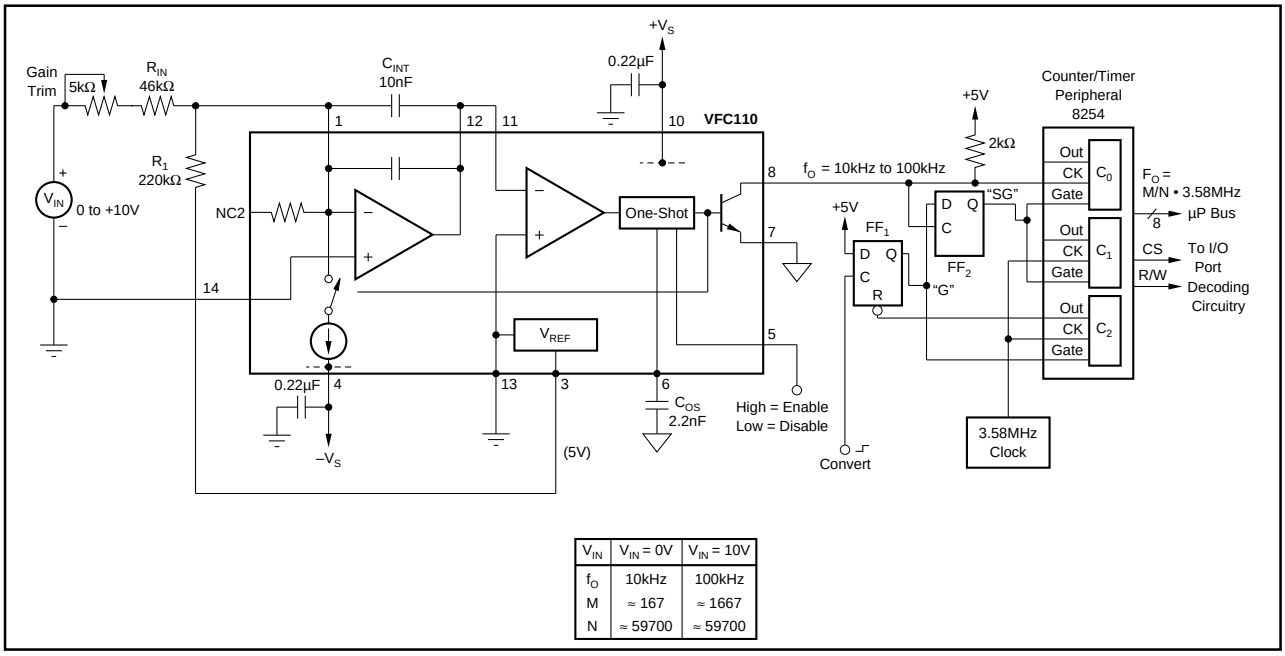


FIGURE 2. The Ratiometric Counting Scheme in This Simplified Diagram Synchronized a Gate Period to the Unknown Input Frequency from the VFC. The synchronized gate is then used to count the high frequency reference. The ratio of the exact count of M VFC pulses and the reference count, N, provide a more accurate measure of the unknown frequency.



V_{IN}	V_{IN} = 0V	V_{IN} = 10V
f_O	10kHz	100kHz
M	≈ 167	≈ 1667
N	≈ 59700	≈ 59700

FIGURE 3. The VFC Input is Offset in this Practical Example so that Low Input Can Be Converted in Short Times. Now the N count always remains near 59,700 over the full input range, while the M count ranges from 167 to 1667.

"G" to an integer number of VFC pulses, creating the synchronized gate "SG" Counter. C0 tallies the exact number (M) of VFC pulses, while C1 simultaneously counts N high speed clock pulses.

Conversion to a digital result is completed by reading the contents of counters C0 and C1 by the microprocessor. The VFC frequency is computed in software as the ratio of M and N times the clock frequency. The proper choice of counter modes programmed in the setup of the 8254 peripheral allows counters C0 and C1 to be automatically reset at the initiation of the next conversion cycle. The Convert command can be created by hardware timing or other peripheral hardware can be used to initiate the conversion process with software control.

The seemingly odd gate period time of 16.66ms has a definite purpose. Since the integration period of the VFC is equal to the counting period, an interfering signal can be rejected by counting for one period (or an integer number of periods) of the interfering signal. Line frequency noise (60Hz) can thus be rejected by counting for 1/60 second or 16.66ms. Figure 4 shows the noise rejection of an A/D converter with an integrating (counting) period of T as a function of frequency. Using a gate period of 16.66ms, the deep nulls in the response curve align with the fundamental and all harmonics of 60Hz. The shorter gate periods feasible with ratiometric counting make the precise choice of the gate period important if good line frequency rejection is to be achieved. With long gate times the line frequency noise is far down the attenuation slope where reasonable noise integration is achieved without great concern as to the precise gate period. Since the actual counting period is determined by the synchronized gate, SG, actual gate times will depend on the input VFC frequency and how the pulses randomly align with the gate. Worst case, however, occurs at low input voltage where the maximum deviation of the synchronized gate time from desired 16.66ms to equal to one period of the VFC at 10kHz or 0.1ms. Even this worst-case deviation from the ideal gate period still yields over 40dB rejection of 60Hz and its harmonics.

Conversion data is available 16.66ms after a convert command is issued, yet the counter resolution is one part in

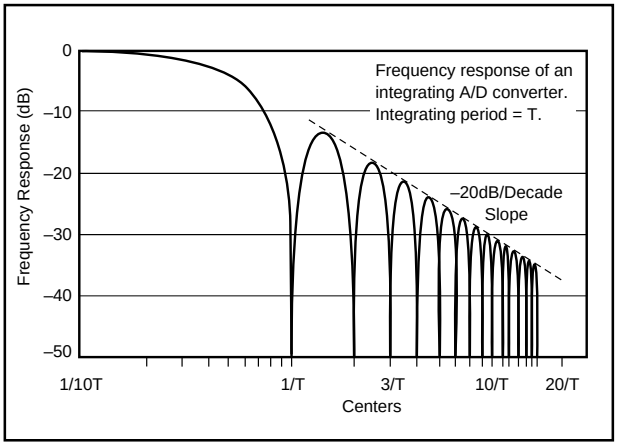


FIGURE 4. The Frequency Response of an Integrating A/D Converter Exhibits a Comb Filter Response. The deep nulls in the response are very useful for rejecting a known interfering signal and its harmonics.

59,667. Using standard counting, it would take 0.5 second to achieve the same resolution.

In principle, the resolution which can be achieved with ratiometric counting can be improved simply by increasing the frequency of the 3.58MHz reference clock. For the same 16.7ms counting period, a higher reference frequency would produce a correspondingly larger number of N counts, increasing the resolution of the result. (The 8254 is limited to 16 bits per counter, but counters could be cascaded for more resolution.) At some point, however, frequency noise (jitter) in the output of the VFC will limit the useful resolution of the result. At this point, counting with greater resolution will produce results which vary from conversion to conversion, affected by random jitter of the VFC.

Figure 5 shows the count repeatability due to frequency noise for a typical VFC110 as measured with a high-speed counter. It shows the repeatability for a 16.66ms counter gate time to be better than 18 bits—consistent with the 16 bit count used in this example.

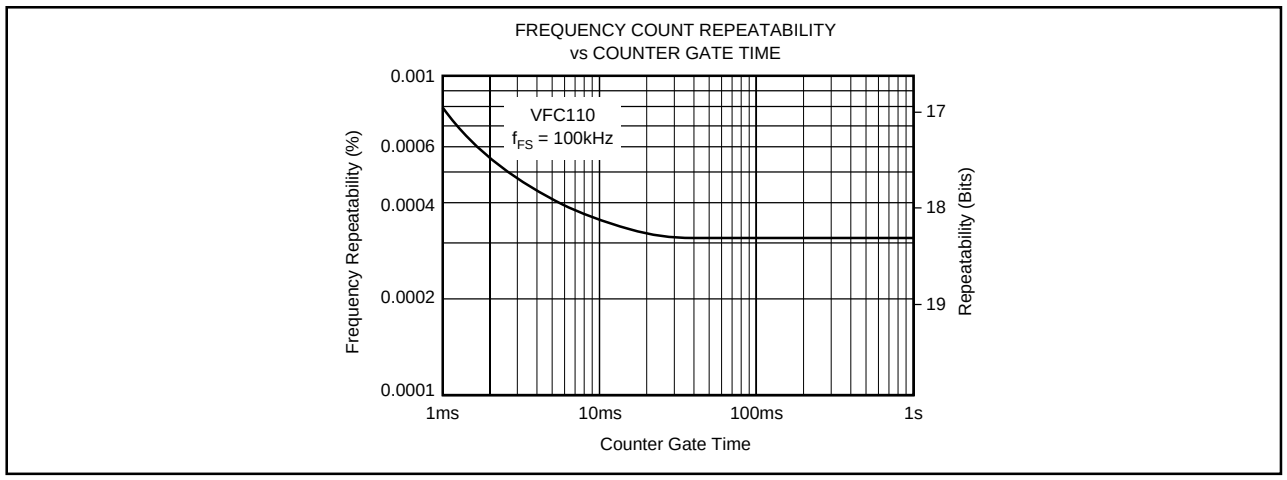


FIGURE 5.

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